Remarks

The Examiner has rejected applicants' claims 1-7, 12, 13, 15-18 and 22 under 35 USC 103(a) as unpatentable over the Izumi, et al. patent (US Patent No. 6,160,673) taken in view of the Twitchell, et al. patent (US Patent No. 6,281,936) in further view of the Sasaki et al. patent (US Patent No. 5,774,290). Claims 8, 9 and 11 have been rejected under 35 USC 103(a) based on the latter patents taken with the Williams patent (US Patent No. 6,344,749). Finally, claim 14 has been rejected under 35 USC 103(a) based on the Izumi, et al., Twitchell, et al. and Sasaki et al. patents taken with the Limberg, et al. patent (US Patent No. 6,426,780). These rejections are respectfully traversed.

Applicants' independent claim 1 recites a reproducing apparatus, comprising: reproducing means for reproducing an information signal; equalizing means for controlling a group delay of the information signal reproduced by said reproducing means; converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of a plurality of bits per sample; detecting means for converting the digital signal output from said converting means into a n-values signal per sample; and control means for controlling a group delay characteristic of said equalizing means by using the digital signal to be input to said detecting means and the n-values signal output from said detecting means. Independent claim 16 has similar features.

The Examiner has argued that the Izumi et al. patent discloses a reproducing apparatus comprising reproducing means for reproducing an information signal (FIG. 5, Col. 11, line 38-48), equalizing means for controlling a group delay of the information signal reproduced by the reproducing means (FIG. 5, Col. 11, lines 38+), detecting means

for detecting a digital signal from the information signal reproduced by the reproducing means (FIG. 1, reproduction amplifier 3 as described in Col. 11, line 38-48) and control means for controlling a group delay characteristic of the equalizing means by using the reproduced information signal to be inputted to the detecting means and a detection result of the detecting means (FIG. 5, Col. 11, lines 38-48). The Examiner has acknowledged that the Izumi, et al. patent fails to disclose a converting means for sampling the information signal output from the equalizing means and for converting the information signal into a digital signal composed of plurality of bits per sample and detecting means for converting the digital output from the converting means into a n-values signal per sample. The Examiner has, however, argued that the Twitchell, et al. patent teaches a transmission system wherein conversion and equalization of the signal is processed and thereby turns the signal into a digital signal by the A/D converter 80 and further sent to the controller for further processing (FIG. 1). The Examiner has also argued that the Sasaki, et al. patent discloses detecting means for conversion of a digital signal as described in Col. 3, lines 50+ through Col. 4, lines 1-30, and that "[t]he digital signal output from the converts the signal and further processes the signal allowing for a proper detection and reproduction of the signal."

Applicants have reviewed the Izumi, et al., Twitchell, et al., and Sasaki, et al. references cited by the Examiner and believe that there is no teaching or suggestion in these references of the combination of : converting means for sampling the information signal output from said equalizing means and for converting the information signal into a digital signal composed of a plurality of bits per sample; detecting means for converting a digital signal output from the converting means into a n-values signal per sample, and

control means for controlling a group delay characteristic of the equalizing means by using digital signal to be input to the detecting means and the n-values signal output from the detecting means. In particular, as acknowledged by the Examiner, the Izumi, et al. patent does not disclose a detecting means that converts the digital signal output from the converting means into a n-values signal per sample. Instead, Izumi, et al. merely discloses a reproduction amplifier (3, or signal detecting means) that detects and amplifies the digital signal recorded on a recording medium and outputs a first reproduction signal. See, Col. 11, lines 38-48. The function of the reproduction amplifier in Izumi, et al., i.e. to detect and amplify recorded signal, is completely different from the function of the detecting means, as recited in applicants' independent claims 1 and 16, i.e. converting digital signal into a n-values signal per sample. Therefore, the reproduction amplifier in Izumi, et al. is in no way equivalent to the detecting means in applicants' claims 1 and 16, and the Izumi, et al. patent does not teach or suggest the detecting means element recited in applicants' claims 1 and 16.

Since the Izumi, et al. patent fails to disclose the detecting means of applicants' independent claims 1 and 16, the Izumi, et al. patent does not, and cannot, teach or suggest using the digital signal to be input to the detecting means and a n-values signal output by the detecting means to control a group delay characteristic of the equalizing means. Moreover, even if the reproduction amplifier of Izumi, et al. could be equated to the detecting means of applicant's claims 1 and 16, there is no mention in Izumi, et al. of using the digital signal to be input to the reproduction amplifier and the signal output by the reproduction amplifier for controlling the equalizing means, i.e., a fixed form equalizing circuit (4 in FIG. 5) which provides phase and amplitude compensation.

Rather, the Izumi, et al. patent only discloses that the fixed waveform equalizing circuit (4 in FIG. 5) receives the amplified signal from the reproduction amplifier, i.e. the first reproduction signal, compensates the phase and amplitude of this signal and outputs the second reproduction signal. See, Col. 11, lines 46-59. The equalizing circuit 4 in Izumi, et al. is fixed and there is no disclosure in Izumi, et al. of any control of the equalizing circuit using the signals input into and output from the reproduction amplifier.

Moreover, the automatic waveform equalizer circuit 63 in the Izumi, et al. patent equalizes the amplitude of the reproduced signal and not the group delay. Thus, the control circuit 64 for controlling the waveform equalizer in the Izumi, et al. patent cannot be equated to applicants' claimed control means for controlling a group delay characteristic of the equalizing means by using digital signal to be input to the detecting means and the n-values signal output from the detecting means.

The Sasaki, et al. patent also does not teach or suggest the detecting means for converting the digital signal into a n-values signal per sample and control means for controlling a group delay characteristic of the equalizing means by using the digital signal to be input to the detecting means and the n-values signal output from the detecting means. In particular, the Sasaki, et al. patent discloses an apparatus having an A/D converter (6 in FIG. 2) which performs sampling of a reproduced signal equalized by an equalizing circuit (5 in FIG. 2) and converts the reproduced signal into a digital signal consisting of a plurality of bits per sample, which is then outputted to a clock-signal generating circuit (14 in FIG. 2) and to a delay circuit (7 in FIG. 2). See, FIG. 2 and Col. 3, lines 50-64. The Sasaki, et al. patent further discloses that the clock-signal generating circuit generates a clock signal for use in the A/D converter, while the delay circuit

delays the signal for a period of two clock signals, a subtracter (8 in FIG. 2) subtracts the original digital signal from the delayed digital signal and the signal is then restored to a two-level signal represented by 1 and 0 by a Viterbi decoding circuit (9 in FIG. 2). See, Col. 3, lines 50-67.

There is no mention in Sasaki, et al. of using the signal to be inputted to the A/D converter (detecting means) and a signal outputted from the A/D converter (detecting means) to control the equalizing circuit, and in particular, using these signals for controlling the group delay of characteristic of the equalizing circuit. Instead, the Sasaki, et al, patent is concerned with generating a clock-signal phase-synchronized with a reproduced signal, which uses the digital signal outputted by the A/D converter only, and is not at all related to controlling an equalizing characteristic of the equalizing circuit.

Applicants therefore submit that, since the Sasaki, et al. patent is not at all concerned with control of an equalizing characteristic, there is no apparent reason for one of skill in the art to use this patent to modify the structure of the Izumi, et al. patent. Moreover, even if such a combination could be made neither the Izumi, et al. nor the Sasaki, et al. patents teach or suggest the detecting means for converting the digital signal output from the converting means into n-values signal per sample and the control means for controlling a group delay characteristic of the equalizing means by using the digital signal to be input to the detecting means and the n-values signal output from the detecting means.

The cited Twitchell, et al. patent also fails to add anything to the Izumi, et al. and Sasaki, et al. patents to result in applicants' claimed invention. Firstly, the Twitchell, et al. patent does not deal with equalizing a signal in a reproducing apparatus, unlike the

system of the Izumi, et al. patent. In particular, the system of the Twitchell, et al. patent is designed to achieve a totally different goal from that being achieved in the Izumi, et al. patent. Specifically, the Twitchell, et al patent system is designed to modify a signal to compensate for distortion caused by amplifier 20 and filters 32 and 38 (which are used within the DTV system when transmitting the signal), beforehand by an equalizer located upstream of the amplifier and the filters.

Therefore, as with the Sasaki, et al. patent, there would be no apparent reason for a person skilled in the art to combine the system of Twitchell, et al. patent with the system of the Izumi, et al. patent.

Moreover, even if the systems could be combined they would still not result in applicants' claimed invention. Thus, the Twitchell, et al. patent was cited for it showing of use of the output from the A/D converter 80 in the controller 60 of the system. However, like the Izumi, et al. patent, there is nothing said in this patent as to converting the output from A/D converter 80 into an n-values signal nor is there a structure to control an equalizing characteristic using the n-values signal.

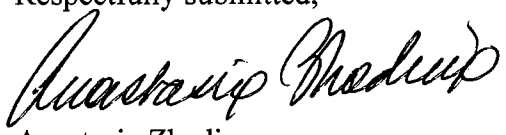
Accordingly, applicants' independent claims 1 and 16, which recite the above features, and their respective dependent claims, patentably distinguish over the Izumi, et al., Twitchell, et al. and Sasaki, et al. patents, taken alone or in combination. Moreover, there is nothing added by the Williams and the Limberg, et al. patents to change this conclusion.

In view of the above, it is submitted that applicants' claims patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is

respectfully requested.

Dated: August 6, 2007

Respectfully submitted,



COWAN, LIEBOWITZ & LATMAN, P.C.
1133 Avenue of the Americas
New York, New York 10036-6799
T: (212) 790-9200

Anastasia Zhadina
Reg. No. 48,544
Attorney of Record